The gm/ID Methodology, a sizing tool for low-voltage analog CMOS Circuits: The semi-empirical and compact model approaches (Analog Circuits and Signal Processing)

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In 'The gm/ID Methodology, a Sizing Tool for Low-Voltage Analog CMOS Circuits', we compare the semi-empirical to the compact model approach. Small numbers of parameters make the compact model attractive for the model paves the way towards analytic expressions unaffordable otherwise. The E.K.V model is a good candidate, but when it comes to short channel devices, compact models are either inaccurate or loose straightforwardness. Because sizing requires basically a reliable large signal representation of MOS transistors, we investigate the potential of the E.K.V model when its parameters are supposed to be bias dependent. The model-driven and semi-empirical methods are compared considering the Intrinsic Gain Stage and a few more complex circuits. A series of MATLAB files found on extras-springer.com allow redoing the tests.

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